

High Speed Signal Layout Course

Abstract

From the very beginnings of electronic design, circuits and systems have been divided into bodies of knowledge: RF (Radio Frequency) and non-RF such as power, analog and digital design. This was a fair practice because the signals on the PCB were low in frequency. But, as the frequency of the signals are now pushed into the hundreds of megahertz and gigahertz ranges, the line separating RF and non-RF no longer holds true. Without taking signal propagation from an RF perspective into consideration, it is very difficult to get HS (high speed) designs to work.

This course is designed to help the PCB designer understand the why, what and how of HS signal propagation by explaining signal propagation from an RF perspective. Typical problems in board layout are discussed and analyzed along with instructions on proper techniques to remedy said problems in order to facilitate the maximum success of signal propagation.

Table of Content

1. Concepts
 - a. E field/ Capacitor
 - b. B field/Inductor
 - c. Transmission line
 - d. Characteristic impedance
 - e. Signals in the frequency domain
 - f. Bandwidth
2. What does “high speed” design really mean?
3. PCB stackup
4. What is dielectric constant and why does it matter?
5. Velocity of propagation

6. Group delay
7. When do you treat a trace as a transmission line?
8. Problem areas
 - a. Stubs - For sinusoids they are bad enough, why are they worse for clocks?
 - b. split planes
 - c. vias
 - d. Dk
 - e. Mismatch
 - f. Common mode distortion
 - g. Package effect
 - h. EMC/EMI
 - i. FCC certification
 - j. Crosstalk
 - i. What is it
 - ii. How it happens
 - k. Loss budget
 - l. PCB Loss
9. Solutions
 - a. stitching capacitors
 - i. Value
 - ii. Placement
 - iii. package
 - b. Vias
 - i. Location
 - ii. Quantity
 - iii. Size
 - iv. Affect
 - c. Length matching
 - i. Intra pair ($\leq 5\text{mil}$)
 1. Why is location important?
 - ii. Tx vs Rx
 - d. End terminations
 - i. When, why and how
 - e. Velocity of propagation
 - i. Dependent on ϵ_r
 - ii. Outside vs inside of PCB

- f. Traces
 - i. Structures
 - ii. Impedance
 - iii. Width and spacing
 - iv. Length
 - v. Length tuning
 - g. When using a power plane as a reference plane
 - i. Why do it?
 - ii. What to look out for
 - iii. Things needed
 - h. Transition locations vs distance (as a function of freq). Any transition should take place where the characteristic impedance is as close to ideal as possible at the frequency of concern.
 - i. Why do you keep seeing “route on top layer” or “on bottom layer”?
 - j. Why avoid 90 degree angles?
 - k. What makes an antenna
 - l. Symmetry vs asymmetry
 - m. $1/r^2$ vs $1/r^3$
10. Summary
- a. Maintain correct impedance over the entire trace
 - b. Minimize impedance mismatch but when unavoidable, create transition.
 - c. Matching lengths between net classes or differential pairs
 - d. Allow enough room for noise aggressors and victims to be far enough apart
 - e. Never split reference planes (but when unavoidable, use stitching capacitors)
 - f. Understand how the dielectric material in the stackup affects everything
 - g. NO stubs